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| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 1 of 18 |

Specification for EE0270AE-1 EPD

Model NO. : EE0270AE-1

| Prepared by | Checked by | Approved by |
|--------------------|-------------------|--------------------|
| | | |

Customer approval

| Customer | Approved by | Date of Approval |
|-----------------|--------------------|-------------------------|
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|------------------|---|----------------------|-------------------|
| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 2 of 18 |

| Version | Content | Date | Producer |
|----------------|----------------|-------------|-----------------|
| V1.0 | New Release | 2019/08/26 | ZHP |
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|------------------|---|----------------------|-------------------|
| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 3 of 18 |

CONTENTS

| | | |
|-------|--|----|
| 1 | General Description..... | 4 |
| 2 | Features..... | 4 |
| 3 | Application..... | 4 |
| 4 | Mechanical Specification..... | 4 |
| 4.1 | Dimension..... | 4 |
| 4.2 | Mechanical Drawing of EPD Module..... | 5 |
| 5 | Input/output Pin Assignment..... | 6 |
| 6 | Electrical Characteristics..... | 7 |
| 6.1 | Absolute Maximum Rating..... | 7 |
| 6.2 | Panel DC Characteristics..... | 7 |
| 6.3 | Panel DC Characteristics(Driver IC Internal Regulators)..... | 8 |
| 6.4 | Panel AC Characteristics..... | 9 |
| 6.4.1 | MCU Interface Selection..... | 9 |
| 6.4.2 | MCU Serial Interface (4-wire SPI)..... | 9 |
| 6.4.3 | MCU Serial Interface (3-wire SPI)..... | 10 |
| 6.4.4 | Interface Timing..... | 10 |
| 7 | Optical Specification..... | 13 |
| 8 | Handling, Safety, and Environment Requirements..... | 14 |
| 9 | Reliability Test..... | 15 |
| 10 | Block Diagram..... | 16 |
| 11 | Typical Application Circuit with SPI Interface..... | 17 |
| 12 | Packaging..... | 18 |
| 13 | Mark and Bar Code Definition..... | 18 |



| | | | |
|------------------|---|----------------------|-------------------|
| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 4 of 18 |

1 General Description

EE0270AE-1 is an Active Matrix Electrophoretic Display(AM EPD), with interface and a reference system design. The 2.7" active area contains 176x264 pixels, and has 2-bit full display capabilities. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2 Features

- ◆ 176×264pixels display
- ◆ White reflectance above 30%
- ◆ Contrast ratio above 8:1
- ◆ Ultra wide viewing angle
- ◆ Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Landscape, portrait modes
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform stored in On-chip OTP
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I²C signal master interface to read external temperature sensor

3 Application

Electronic Shelf Label System

4 Mechanical Specification

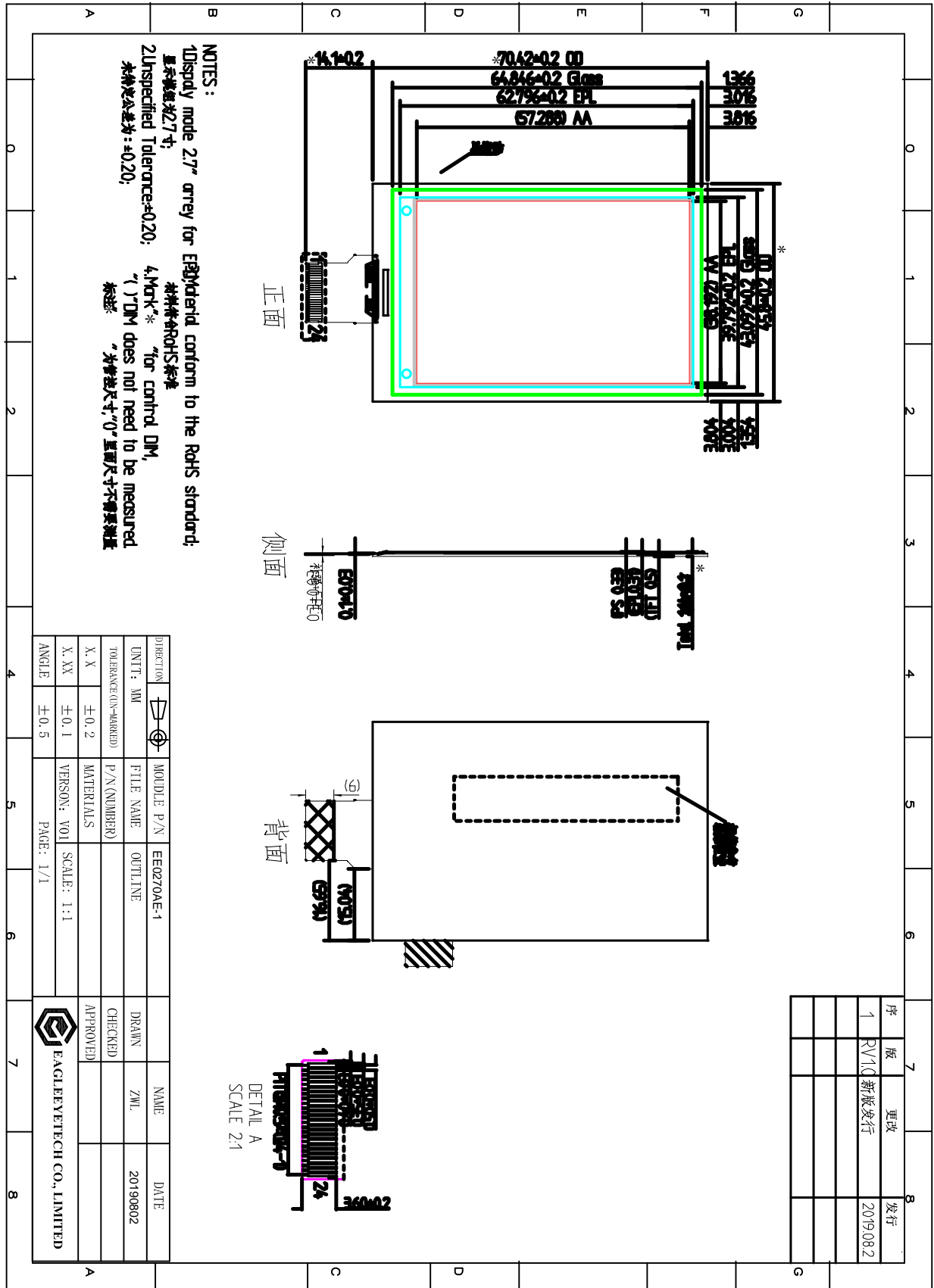
4.1 Dimension

| Parameter | Specifications | Unit |
|---------------------|-----------------------------|-------|
| Screen Size | 2.7 | Inch |
| Display Resolution | 176(H)×264(V) | Pixel |
| Active Area | 38.192×57.288 | mm |
| Pixel Pitch | 0.217×0.217 | mm |
| Pixel Configuration | Rectangle | |
| Outline Dimension | 45.8(H)×70.42 (V) ×1.14 (D) | mm |
| Weight | TBD | g |



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|-----------|----------------------------------|---------------|------------|
| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 5 of 18 |

4.2 Mechanical Drawing of EPD Module





| | | | |
|-----------|----------------------------------|---------------|------------|
| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 6 of 18 |

5 Input/output Pin Assignment

| No. | Name | I/O | Description | Remark |
|-----|-------|-----|---|----------|
| 1 | NC | | Do not connect with other NC pins | |
| 2 | GDR | O | N-Channel MOSFET Gate Drive Control | |
| 3 | RESE | I | Current Sense Input for the Control Loop | |
| 4 | NC | | Do not connect with other NC pins | |
| 5 | VDHR | C | Positive Source driving voltage 1 | |
| 6 | TSCL | O | I ² C Interface to digital temperature sensor Clock pin | |
| 7 | TSDA | I/O | I ² C Interface to digital temperature sensor Data pin | |
| 8 | BS | I | Bus Interface selection pin | Note 5-4 |
| 9 | BUSYN | O | Busy state output pin | Note 5-3 |
| 10 | RSTN | I | Reset signal input. Active Low. | |
| 11 | D/C | I | Data /Command control pin | Note 5-2 |
| 12 | CSB | I | Chip select input pin | Note 5-1 |
| 13 | SCL | I | Serial Clock pin (SPI) | |
| 14 | SDA | I | Serial Data pin (SPI) | |
| 15 | VDD | P | Power Supply for interface logic pins | |
| 16 | VDD | P | Power Supply for the chip | |
| 17 | VSS | P | Ground | |
| 18 | VDDD | C | Core logic power pin VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and VSS under all circumstances | |
| 19 | VPP | P | Power Supply for OTP Programming | |
| 20 | VSH | C | Positive Source driving voltage 2 | |
| 21 | VGH | C | Positive Gate driving voltage | |
| 22 | VSL | C | Negative Source driving voltage | |
| 23 | VGL | C | Negative Gate driving voltage | |
| 24 | VCOM | C | VCOM driving voltage | |

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin



| | | | |
|------------------|---|----------------------|-------------------|
| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 7 of 18 |

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin High when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-4: Bus interface selection pin

| BS State | MCU Interface |
|-----------------|--|
| L | 4-lines serial peripheral interface(SPI) |
| H | 3- lines serial peripheral interface(SPI) - 9 bits SPI |

6 Electrical Characteristics

6.1 Absolute Maximum Rating

| Parameter | Symbol | Rating | Unit |
|----------------------|---------------|------------------------|-------------|
| Logic supply voltage | V_{dd} | -0.5 to +4.0 | V |
| Logic Input voltage | V_{IN} | -0.5 to $V_{dd} + 0.5$ | V |
| Logic Output voltage | V_{OUT} | -0.5 to $V_{dd} + 0.5$ | V |

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: $V_{SS}=0V$, $V_{DD}=3.0V$, $T_{OPR}=25^{\circ}C$.

| Parameter | Symbol | Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|---------------------------|----------------|-------------------|-----------------------|--------------|-------------|--------------|-------------|
| Logic supply voltage | V_{dd} | - | VDD | 2.2 | 3.0 | 3.7 | V |
| High level input voltage | V_{IH} | - | - | $0.8 V_{dd}$ | - | - | V |
| Low level input voltage | V_{IL} | - | - | - | - | $0.2 V_{dd}$ | V |
| High level output voltage | V_{OH} | $IOH = -100\mu A$ | - | $0.9 V_{dd}$ | - | - | V |
| Low level output voltage | V_{OL} | $IOL = 100\mu A$ | - | - | - | $0.1 V_{dd}$ | V |
| OTP Program voltage | V_{PP} | - | VPP | - | 7.5 | - | V |
| Typical power panel | P_{TYP} | - | - | - | 12 | 30 | mW |
| Deep sleep mode | P_{STPY} | - | - | - | 3 | - | uW |
| Typical operating current | I_{opr_VDD} | $V_{dd}=3.0V-$ | - | - | 4.0 | 10 | mA |

| File Name | Specification for EE0270AE-1 EPD | | | Module Number | | EE0270AE-1 | |
|---------------------------------|----------------------------------|--|-----|---------------|----|------------|-----|
| Version | V1.0 | | | Page Number | | 8 of 18 | |
| Sleep mode current | Islp_VDD | VDD=3.0V DC/DC OFF No clock No output load Ram data retain | VDD | - | 20 | -- | uA |
| Deep sleep mode current | IdslpVDD | VDD=3.0V DC/DC OFF No clock No output load Ram data not retain | VDD | - | 1 | -- | uA |
| Operation temperature range | T _{OPR} | - | - | 0 | - | 50 | °C |
| Operation relative humidity | RHop | - | - | - | - | 70 | %RH |
| Operation illuminance intensity | E | indoor only | - | - | - | 2000 | lux |
| Storage temperature range | T _{STG} | - | - | 0 | - | 50 | °C |
| Storage relative humidity | RHst | - | - | 30 | - | 60 | %RH |

Notes: 1. The typical power is measured with following transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Figure 10-2)

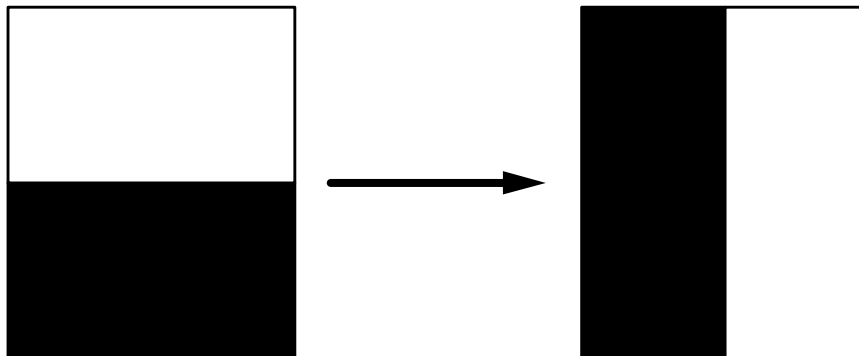


Figure 10-2 The typical power consumption measure pattern

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by EETECH.

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VDD =3.0V, T_{OPR} =25°C.

| Parameter | Symbol | Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|--------------------------------|-----------------|-----------|----------------|-------|------|-------|------|
| VCOM output voltage | VCOM | - | VCOM | -3.0 | - | -0.2 | V |
| Positive Source output voltage | V _{SH} | - | S0-103 | +14.5 | +15 | +15.5 | V |
| Negative Source output voltage | V _{SL} | - | S0-103 | -15.5 | -15 | -14.5 | V |
| Positive gate output voltage | V _{gh} | - | g0-g211 | +21 | +22 | +23 | V |
| Negative gate output voltage | V _{gl} | - | g0-g211 | -21 | -20 | -19 | V |

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|------------------|---|----------------------|-------------------|
| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 9 of 18 |

6.4 Panel AC Characteristics

6.4.1 MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table 10-4-1. Different MCU mode can be set by hardware selection on BS pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

| Pin Name | Data/Connnand Interface | | Control Signal | | |
|------------|-------------------------|------|----------------|-----|------|
| | SDA | SCL | CSB | D/C | RSTN |
| 4-wire SPI | SDIN | SCLK | CSB | D/C | RSTN |
| 3-wire SPI | SDIN | SCLK | CSB | L | RSTN |

Table 10-4-1: MCU interface assignment under different bus interface mode

6.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CSB. In 4-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

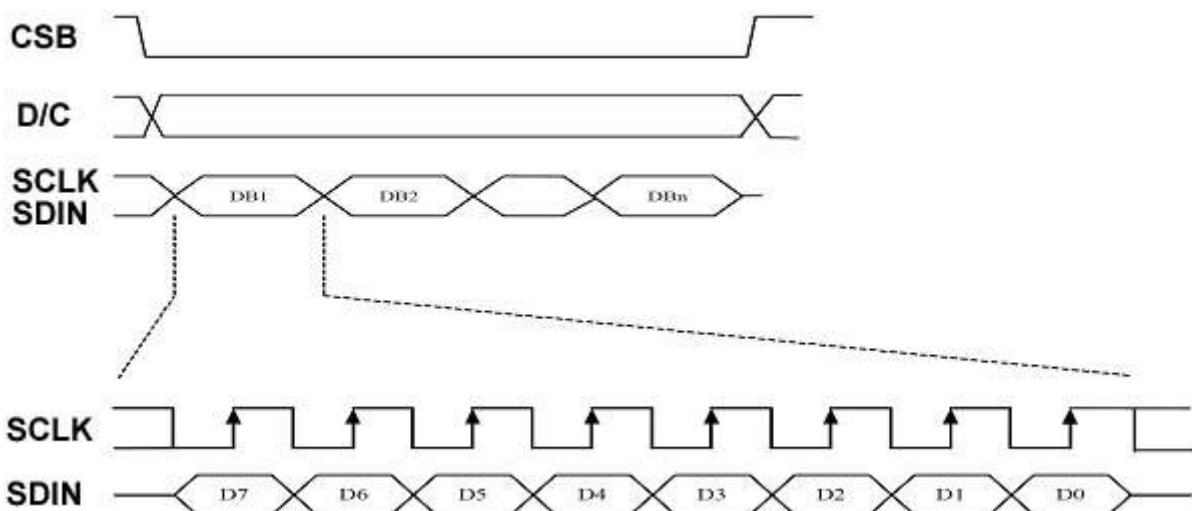
| Function | CSB | D/C | SCLK |
|---------------|-----|-----|------|
| Write command | L | L | ↑ |
| Write data | L | H | ↑ |

Note: ↑ stands for rising edge of signal

Table10-4-2: Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.



| | | | |
|------------------|---|----------------------|-------------------|
| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 10 of 18 |

Figure 10-4-2: Write procedure in 4-wire SPI mode

6.4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB. In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C bit = 1) or the command register (D/C bit = 0).

Under serial mode, only write operations are allowed.

| Function | CSB | D/C | SCLK |
|---------------|-----|-----|------|
| Write command | L | Tie | ↑ |
| Write data | L | Tie | ↑ |

Note: ↑ stands for rising edge of signal

Table 10-4-3: Control pins of 3-wire Serial interface

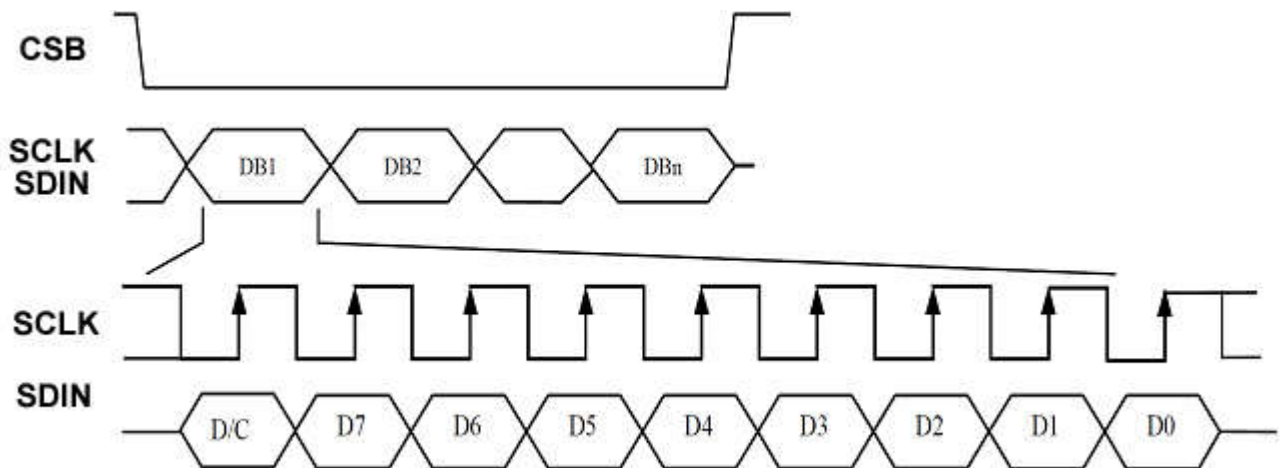


Figure 10-4-3: Write procedure in 3-wire SPI mode

6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VDD =3.0V, T_{OPR} =25°C.

| Symbol | Parameter | Test Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|--------|-------------------------------|------------------|----------------|------|------|------|------|
| Fosc | Internal Oscillator frequency | VDD =2.4 to 3.3V | CL | 0.95 | 1 | 1.05 | MHz |

| | | | |
|------------------|---|----------------------|-------------------|
| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 11 of 18 |

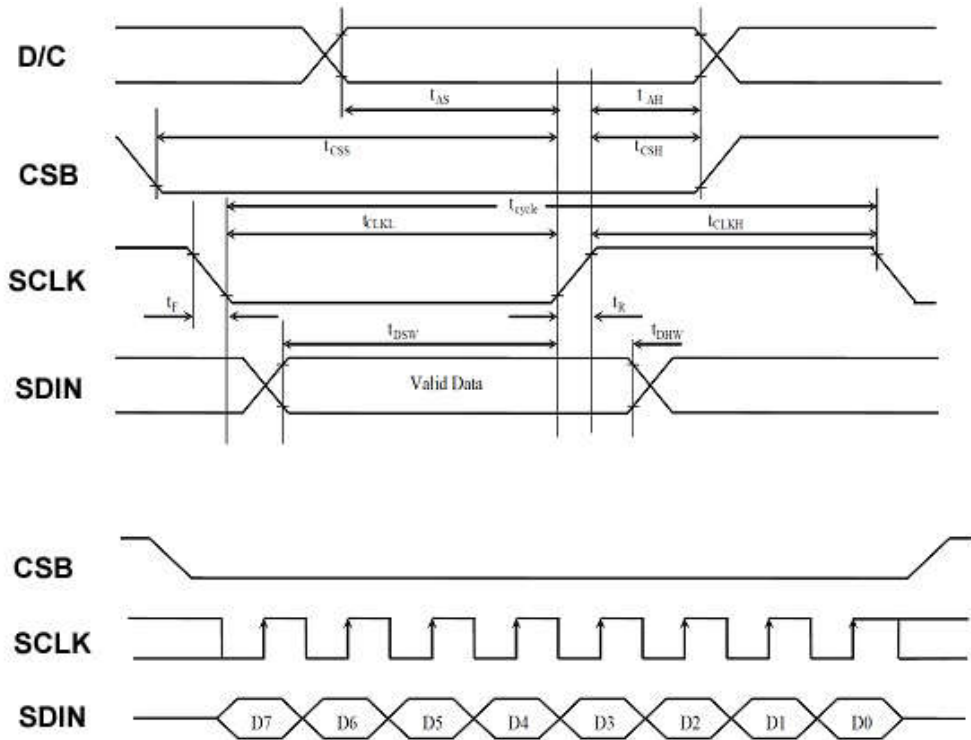


Figure 10-4-4: Serial interface characteristics

($V_{dd} - V_{SS} = 2.4V$ to $3.3V$, $T_{OPR} = 25^{\circ}C$, $CL=20pF$)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-------------|------------------------|------|------|------|------|
| t_{cycle} | Clock Cycle Time | 250 | - | - | ns |
| t_{AS} | Address Setup Time | 150 | - | - | ns |
| t_{AH} | Address Hold Time | 150 | - | - | ns |
| t_{CSS} | Chip Select Setup Time | 120 | - | - | ns |
| t_{CSH} | Chip Select Hold Time | 60 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 50 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 15 | - | - | ns |
| t_{CLKL} | Clock Low Time | 100 | - | - | ns |
| t_{CLKH} | Clock High Time | 100 | - | - | ns |
| t_R | Rise Time [20% ~ 80%] | - | - | 15 | ns |
| t_F | Fall Time [20% ~ 80%] | - | - | 15 | ns |



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| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 12 of 18 |

Table 10-4-4: Serial Interface Timing Characteristics



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|------------------|---|----------------------|-------------------|
| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 13 of 18 |

7 Optical Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

| Symbol | Parameter | Conditions | Values | | | Units | Notes |
|----------------------|--------------------|------------|--------|----------|-----|-------|-------|
| | | | Min. | Typ. | Max | | |
| R | White Reflectivity | White | 30 | 35 | - | % | 11-1 |
| CR | Contrast Ratio | | 8:1 | 10:1 | - | - | 11-2 |
| White Δ L 24h | Reduce | | - | ≤ 4 | - | - | - |
| T _{update} | Image update time | at 25 °C | - | 2100 | - | ms | - |

Notes: 11-1. Luminance meter: Eye-One Pro Spectrophotometer.

11-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.



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| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 14 of 18 |

8 Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.



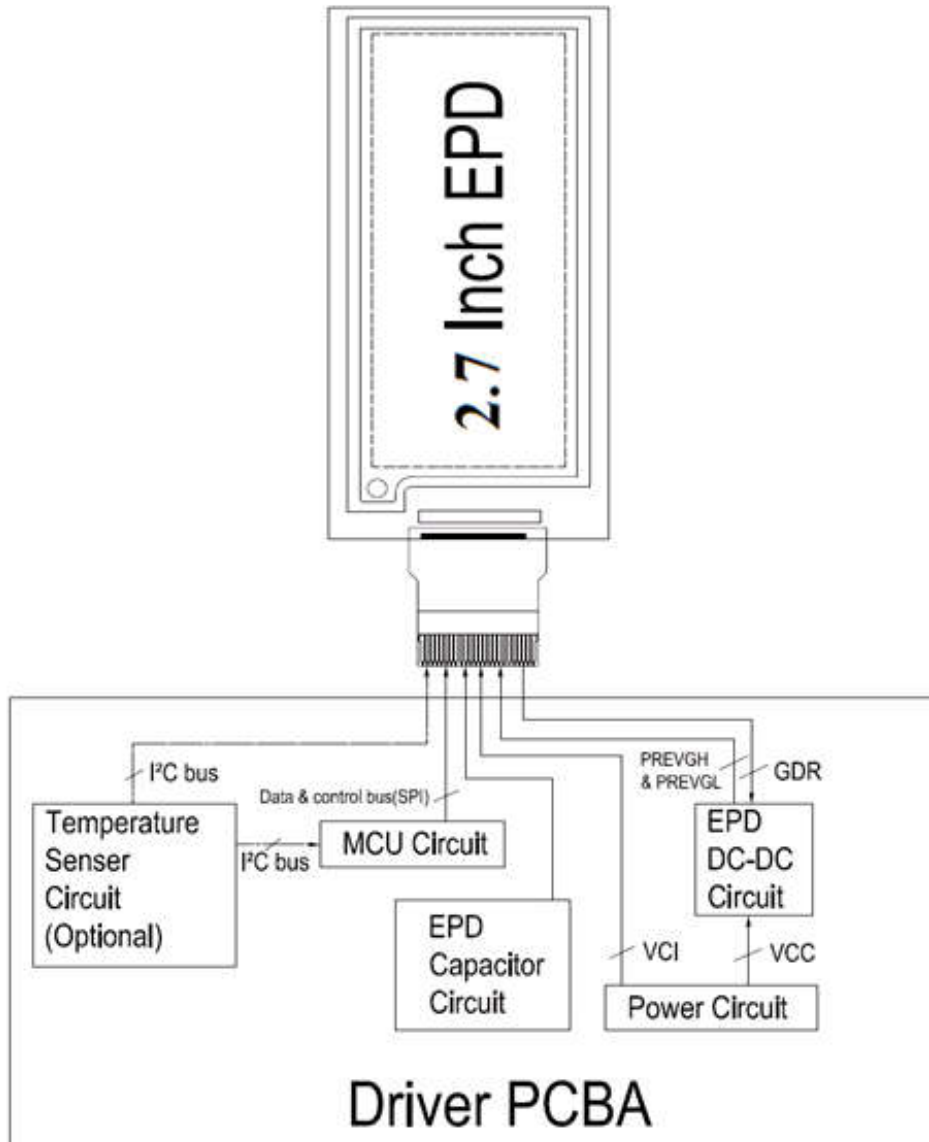
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| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 15 of 18 |

9 Reliability Test

| No. | Test | Condition | Method | Remark |
|-----|---|---|--------------------------|--|
| 1 | High-Temperature Operation | T = +50°C, RH = 30% for 240 hrs | IEC 60 068-2-2Bp | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 2 | Low-Temperature Operation | T = 0°C for 240 hrs | IEC 60 068-2-2Ab | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 3 | High-Temperature Storage | T = +70°C, RH=23% for 240 hrs | IEC 60 068-2-2Bp | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 4 | Low-Temperature Storage | T = -25°C for 240 hrs | IEC 60 068-2-1Ab | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 5 | High-Temperature, High-Humidity Operation | T = +40°C, RH = 90% for 168 hrs | IEC 60 068-2-3CA | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 6 | High Temperature, High-Humidity Storage | T = +60°C, RH=80% for 240hrs | IEC 60 068-2-3CA | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 7 | Thermal Shock | 1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles | IEC 60 068-2-14 | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 8 | Package Vibration | 1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction | Full packed for shipment | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 9 | Package Drop Impact | Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each | Full packed for shipment | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 10 | Electrostatic Effect (non-operating) | Machine model +/- 250V, 0Ω, 200pF | IEC 62179, IEC 62180 | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |

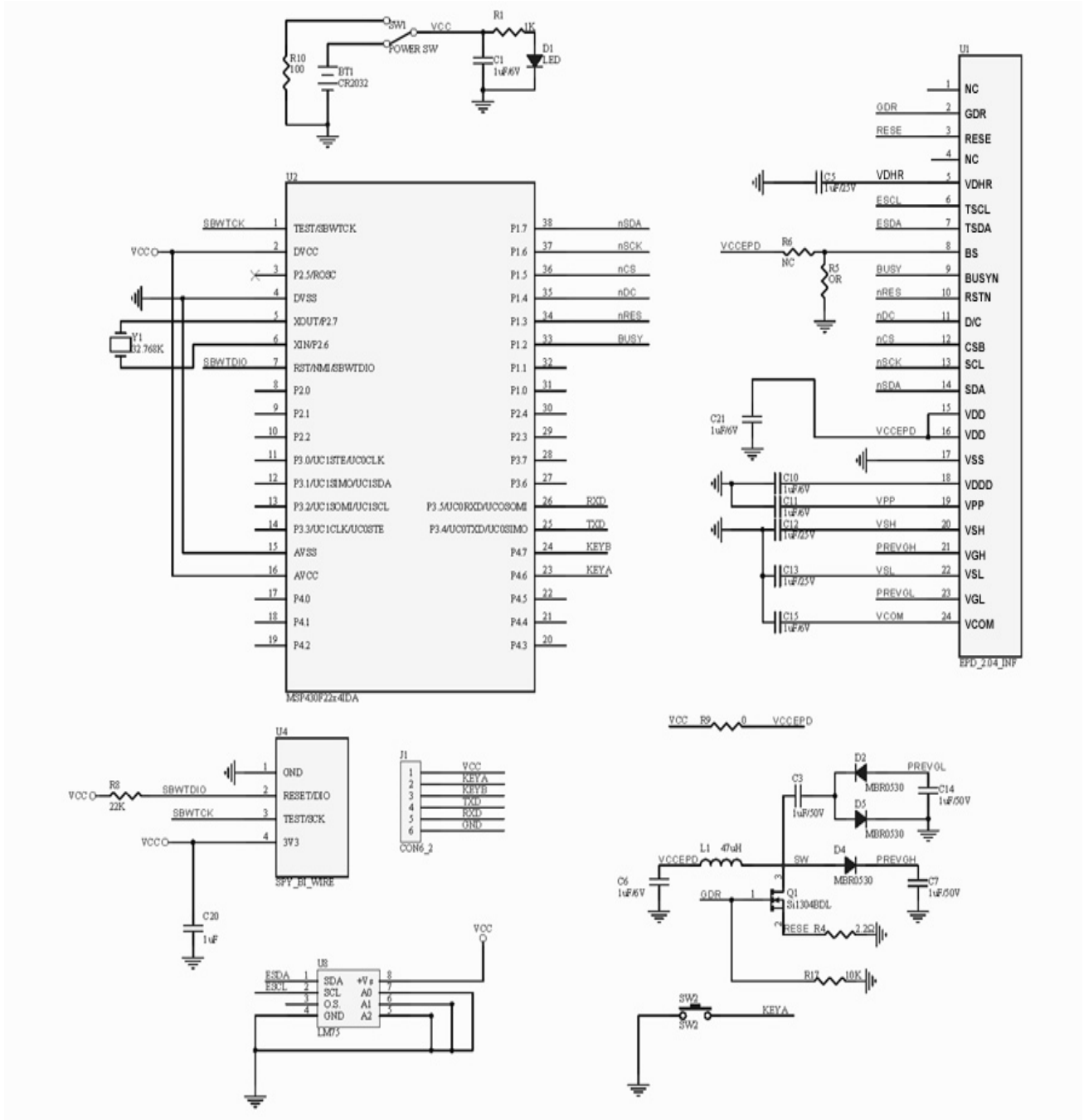
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| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 16 of 18 |

10 Block Diagram



| | | | |
|------------------|---|----------------------|-------------------|
| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 17 of 18 |

11 Typical Application Circuit with SPI Interface





| | | | |
|-----------|----------------------------------|---------------|------------|
| File Name | Specification for EE0270AE-1 EPD | Module Number | EE0270AE-1 |
| Version | V1.0 | Page Number | 18 of 18 |

12 Packaging

TBD

13 Mark and Bar Code Definition

EE0270AE-1 MMMMMMMM XX



R5F086AN1001001

(A) EE0270AE-1: Module No.

(B) MMMMMMMM: Product date year month day

(C) XX: Internal Code

(D) Bar Code definition

R5F086 A N 1 001 001

(1) (2) (3) (4) (5) (6)

(1) O-Paper Film LOT

(2) Factory

(3) Internal Code

(4) Internal Code

(5) Product LOT

(6) Product Serial Number